Department of Electronics & Communication Engineering
राष्ट्रीय प्रौद्योगिकी संस्थान,मणिपुर
NATIONAL INSTITUTE OF TECHNOLOGY MANIPUR
Langol, Imphal – 795 004, Ph. (0385)2445812, e-mail: hodece@nitmanipur.ac.in
(An Autonomous Institute under MHRD, Govt. of India)

PROPOSED SYLLABUS FOR M.TECH INVLSI & EMBEDDED SYSTEM

Program Outcomes (POs) of the M.Tech Program in VLSI and Embedded System:

- Ability to understand the fundamental concepts of electronic circuits, communication systems and computer applications.
- Ability to engage in critical thinking, communicate effectively and demonstrate higher level of professional skills to tackle multidisciplinary and complex problems related to System design using VLSI and Embedded platforms and tools, Semiconductor Technologies.
- Ability to model and offer solutions to issues related to device, IC design, testing and EDA tool development and comprehend the state of the art VLSI technologies.
- Ability to characterize and design analog, digital, RF and mixed signal subsystems meeting given constraints under deep submicron environment.
- Ability to function individually and with teams that are diverse and multidisciplinary, to accomplish a common goal with professional, ethical and social responsibilities.
- Ability to communicate effectively with the community of engineers and the society at large.
- Identify the need for lifelong learning in the context of technological developments.
- Ability to understand the impact of engineering solutions in a global, economic, environmental and social context.

The Programme Educational Objectives (PEOs) are,

1. To equip the masters to have an in-depth knowledge along with new technical ideas, to analyze and evaluate the potential engineering problems and to contribute to the research and development in the core areas by using modern engineering and IT tools.
2. To demonstrate self – management and teamwork in a collaborative and multidisciplinary arena.
3. To inculcate good professional practices with a responsibility to contribute to sustainable development of society.
4. To have a zeal for improving technical competency by continuous and corrective learning.

The Programme Specific Objectives (PSOs) are,

1. To design and develop electronic systems which optimize power and area requirements, free from faults and dependencies by modeling, simulation and testing.
2. To develop electronic systems by learning advanced algorithms, architectures and software – hardware co – design.
3. To communicate engineering concepts effectively by exhibiting high standards of technical presentations and scientific documentations.

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PROPOSED SYLLABUS FOR M.TECH. IN VLSI AND EMBEDDED SYSTEM

SEMESTER-I

Course Code	Course Title	L	T	P	C
VL 501	Analog and Digital CMOS IC Design	3	0	0	6
VL 503	Embedded Systems Design	3	0	0	6
VL 505	Semiconductor Device Modeling	3	0	0	6
VL 507	VLSI System Design	3	0	0	6
VL 5xx	Elective-I	3	0	0	6
VL 53x	Elective-II	0	0	3	3
		Total:			33

SEMESTER-II

Course Code	Course Title	L	T	P	C
VL 502	Semiconductor IC technology	3	0	0	6
VL 504	Low Power VLSI	3	0	0	6
VL 506	Real Time Operating System	3	0	0	6
VL 5xx	Elective-III	3	0	0	6
VL 53x	Elective-IV	0	0	3	3
		Total:			27

SEMESTER-III

Course Code	Course Title	L	T	P	C
VL 621	Project-I	0	0	24	24
		Total:			24

SEMESTER-IV

Course Code	Course Title	L	T	P	C
VL 622	Project-II	0	0	24	24
		Total:			24

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M.Tech in VLSI and Embedded System

Electives-I

Course Code	Course Title	L	T	P	C
VL 521	Digital System Design	3	0	0	6
VL 523	Signal Processing for Embedded Systems	3	0	0	6
VL 525	Microcontroller for Embedded Systems	3	0	0	6
VL 527	Embedded Networking	3	0	0	6
VL 529	FPGA Design	3	0	0	6
VL 531	VLSIDSP	3	0	0	6
VL 535	Digital IC Design	3	0	0	6
VL 537	MEMS and Microsystem Technology	3	0	0	6
VL 539	Biomedical Signal and Systems	3	0	0	6

Electives-II

Course Code	Course Title	L	T	P	C
VL 511	VLSI and Embedded Lab-I	0	0	3	3
VL 513	Signal and Image Processing Lab	0	0	3	3

Electives-III

Course Code	Course Title	L	T	P	C
VL 524	ASIC Design and Modeling	3	0	0	6
VL 526	Embedded Computing	3	0	0	6
VL 528	VLSI EDA Tools	3	0	0	6
VL 530	Reconfigurable Computing	3	0	0	6
VL 532	Memory Technologies	3	0	0	6
VL 534	Filter Design	3	0	0	6
VL 536	CPLD & FPGA Architecture	3	0	0	6

Electives-IV

Course Code	Course Title	L	T	P	C
VL 512	VLSI and Embedded Lab-II	0	0	3	3
VL 514	System Simulation Lab-A	0	0	3	3

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Detailed Syllabus and Course Outcomes

VL 501	Analog and Digital CMOS IC Design	3	0	0	6
Course Outcome	VL 501.1: Able to carry out research and development in the area of analog and digital CMOS IC design. VL 501.2: Design various combinational and sequential Circuits using CMOS logic. VL 501.3 To be well versed with the MOS fundamentals, small signal models,large signal models and analysis of MOSFET based circuits. VL 501.4: Obtain the design of the biasing circuits for CMOS amplifiers. VL 501.5: Able to analyze and design analog circuits such as Differential Amplifier, OP-AMP, Current mirrors, Current amplifiers, Cascode amplifiers, Biasing circuits.				
	MOS Switch, MOS Diode/ Active Resistor, Current Sinks & Sources, Current Mirror, Current & Voltage Reference, Band gap References. Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifier Architectures. Buffered Opamp, High Speed/Frequency Opamps, Differential Output Opamps, Micro power Op amps, Low Noise Opamp. Low Voltage Opamp, Macro models for Opamps. Sequential Circuits. Design of FSM, Moore & Mealy machines, Metastability, Solutions to metastability, Synchronization methods, VHDL codes for complex sequential machines, Hazards, Types of hazards, Method to eliminate hazards, case studies. CMOS parasitic, Technology scaling, Lambda parameter, Design calculations for different logic ckts, Calculations for Area on chip, Power dissipation, PDP, Transmission gate, Domino logic, NORA logic, CMOS layout techniques, Transient response, Advance trends of elements & Alloys for ultra fast logic circuits. **Texts :** 1. J.M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, 2nd ed., PHI, 2003 2. N.H.E. Weste and K. Eshraghian, Principles of CMOS VLSI Design – a System Perspective, 2nd ed., Pearson Education Asia, 2002 3. S.M. Kang and Y. Leblevici, CMOS Digital Integrated Circuits Analysis and Design, 3rd ed., McGraw Hill, 2003 4. J. P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons (Asia) Pte Ltd, 2002 5. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, IEEE Press, 1997. 6. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill 2001 7. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd edition, Oxford University Press, 1997 8. B. Razavi, RF Microelectronics, Prentice-Hall, 1998. 9. P. R. Gray and R. G. Meyer, Analysis and design of Analog Integrated circuits 4th Edition, Wiley Student Edition, 2001. 10. D. A. Johns and K. Martin, Analog Integrated Circuit Design, Wiley Student Edition, 2002.				

VL 502	Semiconductor IC technology	3	0	0	6
Course Outcome	VL 502.1:Acquire knowledge about physics involved in modelling of semiconductor device. VL 502.2: Learn the basics theory of Crystal Growth and Wafer Preparation. VL 502.3: Study the Epitaxy, Diffusion, Oxidation, Lithography and Etching. VL 502.4: Understand the basic steps of fabrication of semiconductor devices.				
	Historical perspective, processing overview, crystal growth, wafer fabrication and basic properties of Silicon Wafers, Clean Rooms, Wafer Cleaning, Epitaxy, Thermal Oxidation of Silicon, Lithography, Wet and Dry Etching, Thin film deposition, Diffusion, Ion Implantation, Metallization, Process Integration: Passive components, Bipolar Technology, MOSFET Technology, MESFET Technology, MEMS Technology, IC Manufacturing: Electrical Testing, Packaging, Yield, Future trends and Challenges: Challenges for integration, system on chip. **Texts:** 1. G. S. May and S. M. Sze, Fundamentals of Semiconductor Fabrication, Wiley India, 2004. 2. J. D. Plummer, M. D. Deal and P. B. Griffin, Silicon VLSI Technology, Fundamentals, Practice and Modeling, Pearson education, 2000. 3. S. M. Sze, VLSI Technology, 2nd Edn., TMH, 2004. 4. S. M. Sze, Semiconductor Devices: Physics and Technology, 2nd Edn., Wiley India, 2011. 5. W. R. Runyan and K. E. Bean, Semiconductor Integrated Circuit Processing Technology, Addison Wesley Publishing Company, 1990. 6. S. A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 1996. 7. M. J. Madou, Fundamentals of Micro fabrication, 2nd Edition, CRC Press, 2011.				
VL 503	Embedded Systems Design	3	1	0	6
Course Outcome	VL 503.1: Understand hardware and software design requirements of embedded systems. VL 503.2: Describe the differences between the general computing system and the embedded system VL 503.3: Develop familiarity with tools used to develop in an embedded environment. VL 503.4: Analyze the embedded systems' specification and develop software programs.				
	Digital Systems and Embedded Systems, Design Methodology, Design Metrics, Specialties, Concepts & types of Memory, Cache Memory, Cache mapping techniques, replacement policies, Cache wire Techniques, Cache Impact on system Performance, Integrated Circuits Technologies- Full custom/VLSI, Logic Families, ASICs , PLDs, PALs, CPLDs , FPGA, Packaging and Circuit Boards, Interconnection and Signal Integrity , Differential Signaling. General Purpose Processor, System On chip, Embedded Computer Organization, ARM 7/ARM 9 architecture, ARM Microcontrollers and Processor Cores, Instructions and Data handling, interfacing with Memory, Interrupts, Timers, ARM Bus. I/O Devices, Controllers, Simple & Autonomous I/O Controllers, Parallel, Multiplexed, Tristate, and Open-Drain Buses, Bus Protocols, Serial Transmission Techniques & Standards, Wireless protocols, CAN & advanced Buses. Design Methodology, Design Flow, Architecture Exploration, Functional Design, Functional Verification, Synthesis, Physical Design, Design Optimization, Area Optimization, Timing Optimization, Power Optimization, Design for Test , Fault Models and Fault Simulation, Scan Design and Boundary Scan, Built-In Self Test (BIST), Nontechnical Issues. **Texts/References:** 1. Digital Design: An Embedded Systems Approach Using Verilog, Peter J. Ashenden ELSEVIER, Morgan Kaufmann Publication, 2008. 2. Data books of ARM7/ARM9 J. Staunstrup and W. Wolf, editors, Hardware/Software Co-				

	Design: Principles and Practice, Kluwer Academic Publishers, 1997. 3. G. DeMicheli, R. Ernst, and W. Wolf, editors, Readings in Hardware/Software Co-Design, Academic Press, 2002.				
VL 504	Low Power VLSI	3	0	0	6
Course Outcome	VL 504.1: Analyze and implement various CMOS static logic circuits. VL 504.2: Learn the design of various CMOS Dynamic logic circuits. VL 504.3: Learn the design techniques of low voltage and low power CMOS circuits forvarious applications. VL 504.4: Design and implementation of various structures for low power applications				
	Introduction: Power dissipation analysis, Physics of Power Dissipation in CMOS FET Devices, Dynamic power, Static power Low-power circuit techniques –Voltage scaling and threshold-voltage hurdle in low-power design, Low power design Using Energy Recovery Technique. Advanced Techniques - Low Power CMOS VLSI Design, Low-power circuit level and device level approach. Low-power Analog and digital design issues in weak inversion and strong inversion regions of operation. Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits. **Text/Reference:** 1. Gary Yeap " Practical Low Power Digital VLSI Design",1997. 2. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", 2000.				
VL 505	Semiconductor Device Modeling	3	0	0	6
Course Outcome	VL505.1: Describe the properties of materials and Application of semiconductor electronics VL 505.2: Apply the knowledge of semiconductors to illustrate the functioning of basic electronic devices. VL 505.3: Demonstrate the control Applications using semiconductor devices. VL 505.4: Identify the fabrication methods of integrated circuits.				
	p-n Junctions: equilibrium conditions, forward and reverse-biased junctions, reverse-bias breakdown, transient and a-c conditions, recombination and generation in the transition, semiconductor hetero-junctions, Metalsemiconductor junctions: Schottky barriers, rectifying and Ohmic contacts, Bipolar junction transistors: minority carrier distribution and terminal currents, generalized biasing, switching, secondary effects, frequency limitations of transistors, hetero-junction bipolar transistors, Field-Effect Transistors: JFETcurrent-voltage characteristics, effects in real devices, high-frequency and high-speed issues, Metal Insulator Semiconductor FET, MOSFETbasic operation and fabrication; ideal MOS capacitor; effects of real surfaces; threshold voltages; output and transfer characteristics of MOSFET, short channel and Narrow width effects, MOSFET scaling, Optoelectronics Devices: Light emitting diodes, Lasers, Photoconductors, Junction Photodiodes, Avalanche Photodiodes, Solar Cells, SPICE Models for Semiconductor Devices: MOSFET Level 1, Level 2 and level 3 model, Model parameters; SPICE models of p-n diode and BJT. **Texts:** 1. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Edition, PHI Private Limited, 2011. 2. P. Bhattacharya, Semiconductor Optoelectronics Devices, 2nd Edition, PHI, 2009. 3. G. Massobrio and P. Antognetti, Semiconductor Device Modeling withSPICE, 2nd Edition, TMH, 2010. 4. C. C. Hu, Modern Semiconductor Devices for Integrated Circuits, Pearson Education, 2010. 5. R. S. Muller and T. I. Kamins, Device Electronics for Integrated Circuits, 3rd Edition, Wiley India, 2009. 6. S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd Edition, Wiley India,				

	2010. 7. Y. Tsividis, Operation and Modeling of the MOS transistor, 2nd Edition, TMH, 1999. 8. S. A. Neamen and D. Biswas, Semiconductor Physics and Devices, 4th Edition, TMH, 2012.				
VL 506	Real Time Operating System	3	0	0	6
Course Outcome	VL 506.1:Understand the fundamentals of interaction of OS with a computer and User computation VL 506.2: Recognize how process are created and controlled with OS VL 506.3: Learn the programming logic of modelling Process based on range of OS features VL 506.4: Understand the development of the target system by porting RTOS				
	Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance, Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model,Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II. Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management. **Texts:** 1. µC/OS-II, The real time Kernel, Jean J. Labrossy, Lawrence: R & D Publications, 2000. 2. Embedded Real Time Systems: Concepts, Design & Programming, Dr.K.V.K.K. Prasad, Dreamtech Publication, 2007. 3. An Embedded Software Primer, David E. Simon, Pearson Education Publication, 2005. 4. Modern Operating Systems, Second Edition, Andrew S. Tanenbaum, Prentice Hall Publication, 2001. 5. Embedded Systems Architecture, Programming and design, Raj Kamal, Tata MCgraw-Hill Publication, 1999.				
VL 507	VLSI System Design	3	0	0	6
Course Outcome	VL 507.1: Ability to understand the basics of system hardware design with hierarchical design. VL 507.2: Ability to understand how the system components are interfaced with each other. VL 507.3: Ability to know methods to handle multiple clocks in a system. VL 507.4: Ability to make out differences between synchronous and asynchronous design systems. Designing of FSM and to know different strategies to assign the states.				
	Basics of system hardware design: Hierarchical design using top-down and bottom-up methodology, System partitioning techniques, interfacing between system components, Handling multiple clock domains, Synchronous and asynchronous design styles; Design of finite state machines: state assignment strategies; The Processor: Data path and Control, Enhancing performance with Pipelining, exploiting of Memory hierarchy. **Texts / References:** 1. G. De. Micheli, Synthesis and Optimization of Digital Circuits, Tata McGraw-Hill, 2004. 2. D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 2nd Edition, Morgan Kaufmann Publishers, Inc, 1998. 3. J. Rabaey, Digital Integrated Circuits, A Design Perspective, 2nd Edition, Pearson Education, 2003. 4. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Eight Indian Reprint, Pearson Education, 2002. 5. C. Mead and L. Conway, Introduction to VLSI				

	Systems, Addison Wesley, 1979.

VL 521	Digital System Design	3	0	0	6
Course Outcome	VL 521.1: Design Mealy and Moore finite state machines for the given specifications. VL 521.2: Understand the overview of clock skew concept. VL 521.3: Understand overview of PLDs, CPLDs and FPGAs. VL 521.4:Use hardware description language and logic simulation tools.				
	Principles of Sequential logic design: Concept of FSM - Metastability, State machine structures: Moore machine - Mealy machine, Analysis of state machine with D and J-K Flip-flops, Clocked synchronous state machine design, Designing state machine using state diagrams, State machine synthesis using transition list, Clock skew, Overview of PLDs, CPLDs and FPGAs, RT level combinational circuit, Regular sequential circuit, Design examples with VHDL. **Texts:**1. J. F. Wakerly: Digital Design-Principles and Practices, 4th Edition, Pearson, 2008. 2. Pong P. Chu: FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version, 1st Edition, WileyInterscience, 2008.				
VL 523	Signal Processing for Embedded Systems	3	0	0	6
Course Outcome	VL 523.1: Illustrate various signal processing algorithms and transforms VL 523.2: Organize DSP algorithms using flow graph representations VL 523.3: Integrate transforming techniques like folding/ unfolding, retiming, parallel processing to achieve faster computations and better efficiency VL 523.4: Judge the performance of the algorithms using various DSP processor architectures				
	Digital Signal Processing Overview, Convolution, Correlation, Digital filters, DFT, STFT, DCT, wavelets and filter banks, FFT algorithms and Implementation, Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph, iteration bounds, Pipelining and Parallel processing of FIR filters, Algorithm transformation: Retiming , Folding, Unfolding, Algorithmic strength reduction in Filters and Transforms, Parallel FIR filters, Fast FIR algorithms, Discrete cosine transform and Inverse DCT, Parallel processing for IIR filters, Pipelined adaptive digital filters. Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, real time implementation considerations, Hardware interfacing, DSP processor				

	architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations, Applications of DSP systems: FIR filters, IIR filters, DTMF generation and detection, FFT algorithms, wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction. **Texts:** 1. Sen M. Kuo and Woon-Seng Gan, "Digital Signal Processors, architectures, implementations, and applications", Prentice-Hall, 1999. 2. V. Madisetti, " The Digital Signal Processing Handbook", IEEE press, 2000 3. K. K. Parhi, "VLSI Digital Signal Processing Systems- Design and Implementation", John Wiley & Sons, Inc, 2008. 4. Sanjit K. Mitra, " Digital Signal Processing: A Computer based approach", McCraw Hill, 1998. 5. Lawrence R. Rabiner and Bernard Gold, "Theory and application of Digital signal Processing", Prentice-Hall of India, 2006.				
VL 524	ASIC Design and Modeling	3	0	0	6
Course Outcome	VL 524.1: Describe the design flow, types and the programming technologies of an ASIC and its construction VL 524.2: Describe the goals, objectives, measurements and algorithms of floorplanning & placement then apply those algorithms to place the logic cells inside the flexible blocks of an ASIC to meet the objectives. VL 524.3: Describe the goals, objectives, measurements and algorithms of routing then apply those algorithms to route the channels then describing various circuit extraction formats and investigate the issues and discover solutions in each step of physical design flow of an ASIC. VL 524.4: Design an ASIC for digital circuits with ASIC design flow steps consists of simulation, synthesis, floorplanning, placement, routing, circuit extraction and generate GDSII File for fabrication of an ASIC, then analyze the ASIC to meet the performance in terms of area, speed and power using EDA tools.				
	Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort. PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLSAND PROGRAMMABLE ASIC I/O CELLS 9 Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks. PROGRAMMABLE ASIC ARCHITECUTREArchitecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques. LOGIC SYNTHESIS, PLACEMENT AND ROUTINGLogic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.				
VL 525	Microcontroller for Embedded Systems	3	0	0	6
Course Outcome	VL 525.1: Learn the basic hardware of various microcontrollers VL 5252: Program, build and test a microcontroller system VL 525.3: Interface a microcontroller system to user controls and other electronic systems. VL525.4: Understand the internal architecture of microcontroller systems, including counters, timers, ports, and memory.				
	ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions. Thumb Instruction Set: Register Usage, Other				

	Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops. Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch. **Texts/References**: 1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier. 2. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.				
VL 526	Embedded Computing	3	0	0	6
Course Outcome	VL 526.1: Understand the embedded processor architectures. VL 526.2:Understand the various semiconductor memories including RAM and ROM. VL 526.3:Design and develop a basic embedded system by programming. VL 526.4: Understand the communication protocols used in embedded systems.				
	System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Tasks, Threads, Multi-Threading, Semaphore, Message Queue. GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools. Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with dataprocessing and display, OpenCV for machine vision, Audio signal processing. Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security. Application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools. **Texts/References:** 1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012. 2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998. 3. Assembly Language for x86 Processors by Kip R. Irvine 4. Intel® 64 and IA-32 Architectures Software Developer Manuals 4. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne. 5. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall 6. UNIX Network Programming by W. Richard Stevens				
VL 527	Embedded Networking	3	0	0	6
Course Outcome	VL 527.1: Learn the serial and parallel communication protocol related to embedded networking. VL 527.2: Understand the concepts of USB & CAN bus. VL 527.3: Understand the concepts of Embedded Ethernet. VL 527.4: Recognize the need for wireless protocols to indulge in Real world interfacing.				
	Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire. USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types – Enumeration – Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN. Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and				

	network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol. Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure. Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing. **Texts/ References:** 1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002 2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996. 3. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008. 2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003. 3. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.				
VL 528	VLSI EDA Tools	3	0	0	6
Course Outcome	VL 528.1: Organize the various equipments and components required for VLSI product development. VL 528.2: Survey on the libraries available in the CAD tools. VL 528.3: Identify Algorithms for circuit simulation. VL 528.4: Understand the concepts of high level synthesis.				
	ASIC design flow, various design entries, IP cores, cross compilers, cell design, stick diagrams, synthesis, place and route, floor planning, power estimation, static timing analysis, dynamic timing analysis, antenna rules, design rule check, electric rule check, schematic rule check, Clock domain crossing check, layout verses schematic, layout techniques, verification, manufacturing tests. Xilinx ISE, Actel libero, Active HDL, Sinplify pro, Leonardo spectrum, Quartus, Boole Dozer, Model Simdesign entries, various simulation, synthesis, place and route, timing verification. Cadence, IC station – design entries, simulations, various tools in the suit, GDS files. Microwind, Spice, Magic – layout techniques, simulations, DRCs, tools available in the suit. **Texts:** 1. Michael Smith, “Application Specific Integrated Circuits”, Pearson Education Asia, 2000. 2. Reference manuals of the respective tools.				
VL 529	FPGA Design	3	0	0	6
Course Outcome	VL529.1: Understand design and implementation styles. VL 529.2:Use computer-aided design tools to synthesize, map, place, routing, and download the digital designs on the FPGA board. VL 529.3: Identify and distinguish different special purpose processor architecture. VL 529.4: Understand design of parametrized library cells.				
	Architecture vs organization, Design styles, Implementation styles, Design Examples using programmable logic devices, Design of Universal block. Design of memory, Floating point multiplier, Barrel shifter, Special purposeProcessors - Xilinx Vertex and Spartan - II; Altera FLEX 10k and other architectures. Design of parameterized library cells, Implementation and Testing- Xilinx,Actel and Altera FPGA based systems. Design - Case study. **Texts:** 1. John V.Old Field, Richrad C.Dorf, Field Programmable Gate Arrays, John Wiley1995. 2. Michel John Sebastian Smith: Application Specific Integrated Circuits, Pearson, 1997.				
VL 530	Reconfigurable Computing	3	0	0	6

Course Outcome	VL 530.1: Understand the Concept of Reconfigurable Computing and FPGA Architectures. VL 530.2: Model the digital system building blocks using the HDL Language. VL 530.3: Explore the scope of reconfigurable computing in various applications. VL 530.4: Analyze and optimize the various design parameters.				
	Computing requirements, Area, Technology scaling, Instructions, Custom Computing Machine, Overview, Comparison of Computing Machines. Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories, Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD; Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research; Software challenges in System on chip; Testability challenges; Case studies. Modelling , Temporal portioning algorithms, Online temporal placement, Device space management, Direct communication, Third party communication, Bus based communication, Ckt switching, Network on chip, Dynamic network on chip, Partial reconfigurable design. **Texts:** 1. IEEE Journal papers on Reconfigurable Architectures. 2. "High Performance Computing Architectures" (HPCA) Society papers. 3. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication, 2009. 4. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication, 2011.				
VL 531	VLSI DSP	3	0	0	6
Course Outcome	VL 531.1: Understand the overview of DSP concepts VL 531.2: Perform Pipelining and parallel processing in FIR systems to achieve high speed and low power VL 531.3: Perform retiming, unfolding and folding in FIR and IIR filters. VL 531.4: Understand systolic architecture design for FIR filters VL 531.5: Learn and understand the different techniques of power reduction and power estimation.				
	Introduction to DSP systems: Representation of DSP algorithms; Iteration Bound: Definition, Examples, Algorithms for computing Iteration bound; Pipelining and Parallel Processing: Definitions, Pipelining and parallel processing of FIR filters, Pipelining and parallel processing for low power; Retiming: Definitions and Properties, Solving system of Inequalities, Retiming techniques; Unfolding: Definition, An algorithm for unfolding, Applications of unfolding; Folding: Definition, Folding transformations, Register minimization techniques, Register minimization in folded architectures; Systolic Architecture Design: Introduction, Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-Matrix multiplication and 2D systolic array design; CORDIC based Implementations: Architecture, Implementation of FIR filter and FFT algorithm; Bit-Level arithmetic architectures: Parallel multipliers, Bit-serial multipliers, Bit-Serial FIR filter design and Implementation; Redundant arithmetic: Redundant number representation, Carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures; Low-power design: Theoretical background, Scaling versus power consumption, Power analysis, Power reduction techniques, Power estimation				

	approaches. **Texts:** 1. U. Meyer-Baese, DSP with FPGA, Springer, 2004. 2. K. K. Parhi, VLSI DSP Systems, Wiley, 2003. 3. R.G. Lyons, Understanding Digital Signal Processing, Pearson Education, 2004.				
VL 532	Memory Technologies	3	0	0	6
Course Outcome	VL 532.1: Understand memory architectures of SRAM, DRAM and non-volatile memories. VL 532.2: Understand memory design trade-offs. VL 532.3: Examine memory fault models. VL 532.4: Analyze the various advance memory technologies.				
	Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc. **Texts:** 1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice- Hall of India Private Limited, New Delhi, 1997. 2. Memories", Springer Publication. 3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.				
VL 534	Filter Design	3	0	0	6
	VL 534.1: Learn and understand the basic parameters of signal and its processing methods. VL 534.2: Understand the concepts of different technique of signal processing based on various types of noise. VL 534.3: Understand the concept of various models to analyze the power spectrum. VL 534.4: Understand the concept of various Impulse noise modeling.				
	Signals, Noise and Information, Signal Processing Methods, Transform-Based Signal Processing, Source-Filter Model-Based Signal Processing. Bayesian Statistical Model-Based Signal Processing. Different classes of noises and distortion, Linear prediction models, forward and backward models, Eigenvalue and PCA, power spectrum analysis. Impulse noise modelling, detection and removal. Impulse noise using linear prediction models. **Text/References:** S.V. Vaseghi, Advance signal processing and noise reduction, Wiley, 2008.				
VL 535	Digital IC Design	3	0	0	6
Course Outcome	VL 535.1: Learn the basics modelling and fabrication of CMOS Integrated circuits. VL 535.2: learn the design of power performance tradeoff. VL 535.3: Design and analysis of digital integrated circuits. VL 535.4: Learn the basic digital logic gate and their applications.				

	Introduction; Metrics; Switch Logic; Process; Gates; MOS Transistor; Inverter VTC,MOS Capacitor; Inverter Delay; Power Buffer Sizing; Wires; CMOS Logic; Logical Effort; Process variation Effects, Introduction to VLSI fabrication. Memory; Decoders; Pass Transitor; Dynamic and Static Logic; Domino Logic; Scaling; Adders; Multipiers; Latches; Timing; Clock; SRAM; Design for Performance; Power Performance Tradeoff. Analysis and Design of Digital Integrated Circuits. Circuit analysis of piecewise linear single energy storage element networks. Rules for determining states of diodes and transistors. Bipolar junction and field effect transistors as switches. Basic digital logic gates. Integrated circuit logic and building blocks (TTL, MOS, CMOS, ECL, Integrated Injection Logic). Sweep circuits (constant current, Miller, bootstrap), Monostable, Astable, and Bistable (Schmitt Trigger) switching circuits, Applications (pulse width modulator, triangle wave generator, FM function generator design). **Text/References:** 1. Ivan Sutherland, Robert F Sroull, David Harris, Logical Effort: Designing Fast CMOS Circuits 2. N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985 3. L. Glaser and D. Dobberpuhl, The Design and Analysis of VLSI Circuits, Addison Wesley, 1985 4. C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979. 5. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997				
VL 536	CPLD and FPGA Architecture	3	0	0	6
Course Outcome	VL 536.1: Learn and understand the knowledge of PLDs, FPGA Design and architecture. VL 536.2: Understand the different types of arrays. VL 536.3: Design and analyze the FSM techniques and different case studies. VL 536.4: Design and implementation of various digital circuits using FPGA and its applications.				
	Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices –Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation. Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs. Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures. Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures. General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture. **Text/References:** 1.Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition. 1. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning. 2. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India. 3. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition. 4. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.				

VL 537	MEMS and Microsystem Technology	3	0	0	6
Course Outcome	VL 537.1: Ability to understand the operation of MEMS, micro systems and their applications. VL 537.2: Ability to design the micro devices, micro systems using the MEMS fabrication process. VL 537.3: Gain knowledge of basic approaches for various sensor designs. VL 537.4: Gain knowledge of basic approaches for various actuator designs.				
	Historical Background: Silicon Pressure sensors, Micromachining, MicroElectro Mechanical Systems Microfabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA) Physical Microsensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors Microactuators : Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems : Success Stories, Micromotors, Gear trains, Mechanisms Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays **Text/References:** 1. Stephen D. Senturia, "Microsystem Design" by, Kluwer Academic Publishers, 2001. 2. Marc Madou, “Fundamentals of Microfabrication” by, CRC Press, 1997.Gregory Kovacs, “Micromachined Transducers Sourcebook” WCB McGraw-Hill, Boston, 1998. 3. M.-H. Bao, “Micromechanical Transducers: Pressure sensors, accelerometers, and gyroscopes” by Elsevier, New York, 2000.				
VL 539	Biomedical Signal and Systems	3	0	0	6
Course Outcome	VL 539.1 Understand the origin of biomedical signals and its dynamics VL 539.2 Learn the concept of pre-processing and filtering for removal of artifacts VL 539.3 Understand the methods for event detection and waveform analysis VL 539.4 Develop models for biomedical systems				
	Introduction to Biomedical Signals, Nature of Biomedical Signals, Examples of Biomedical Signals – EMG, ECG, EEG, ERPs, PCG, VMG, VAG, Objectives of Biomedical Signal Analysis, Difficulties in Biomedical Signal Analysis, Concurrent, Coupled, and Correlated Processes- Illustration of the Problem with Case-Studies. Filtering for Removal of Artifacts-Illustration of the Problem with Case-Studies, Time-Domain Filters, Frequency-Domain Filters, Optimal Filtering, The Wiener Filter, Adaptive Filters for Removal of Interference, Selecting an Appropriate Filter Application: Removal of Artifacts in the ECG, Event Detection, Detection of Events and Waves, Correlation Analysis of EEG channels, Cross-spectral Techniques. The Matched Filter, Detection of the P Wave, Homomorphic Filtering, Application- ECG Rhythm Analysis, Identification of Heart Sounds, Wave shape and waveform Complexity, Analysis of Event-related Potentials, Morphological Analysis of ECG Waves, Envelope Extraction and Analysis of Activity, Application- Normal and Ectopic ECG Beats, Analysis of Exercise ECG. Frequency-domain Characterization The Fourier Spectrum, Estimation of the Power Spectral Density Function, Measures Derived				

	form PSDs. Modeling Biomedical Systems, Point Processes Parametric System Modeling Autoregressive of All pole Modeling, Pole-Zero Modeling, Electromechanical Models of Signal Generation, Application- Heart-rate Variability, Spectral Modeling and Analysis of PCG. Analysis of Non stationary Signals, Time-Variant Systems, Fixed Segmentation, Adaptive Segmentation, Use of Adaptive Filters for Segmentation, Application- Adaptive Segmentation of EEG Signals, Adaptive Segmentation of PCG Signals. Pattern Classification and Diagnostic Decision , Pattern Classification, Supervised Pattern Classification, Unsupervised Pattern Classification, Probabilistic Models and Statistical Decision , Logistic regression Analysis The Training and Test Steps, Neural Networks, Measures of Diagnostic Accuracy and Cost, Reliability of Classifier and Decisions **Texts:** 1. R. M. Rangayyan "Biomedical Signal Analysis- A case study approach", Wiley Publications, 2006. 2. Eugene N Bruce "Biomedical signal processing and signal modeling", Wiley publications, 2007.